Atty. Docket No. OG03-042
Serial No: 10/749,843

Remarks

The present invention relates to a method for fabricating a nonvolatile memory device. The method (as set forth in amended Claim 1 above) generally comprises:

a) forming a lower insulating layer and a sacrificial layer on a semiconductor substrate;

b) patterning the sacrificial layer and forming spacers on sidewalls of the sacrificial layer pattern, the spacers comprising polymers resulting from the patterning of the sacrificial layer;

c) removing the exposed lower insulating layer using the sacrificial layer pattern and the spacers as an etching mask to form a lower insulating layer pattern; and

d) removing the sacrificial layer pattern and the spacers.

The references cited against the originally-filed claims (Ahn, U.S. Pat. No. 6,342,451 [hereinafter "Ahn"], Keller, U.S. Pat. No. 5,968,844 [hereinafter "Keller"], and Yu et al., U.S. Pat. No. 5,801,083 [hereinafter "Yu et al."]) neither disclose nor suggest removing an exposed insulating layer using a sacrificial layer pattern and spacers comprising polymers resulting from the patterning of the sacrificial layer as an etching mask (see amended Claim 1 above). Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1, 2 and 4 under 35 U.S.C. § 103

The rejection of Claims 1, 2 and 4 under 35 U.S.C. §103 as being unpatentable over Ahn in view of Keller is respectfully traversed.

Ahn teaches a method of fabricating floating gates in [a] semiconductor device (Title). According to an embodiment of Ahn, floating gates in a semiconductor device are fabricated by first forming a tunnel oxide layer, a polycrystalline silicon layer, an interlayer oxide layer, and a silicon nitride layer sequentially on a semiconductor substrate having isolation regions (col. 2, ll. 51-56). A plurality of silicon nitride layer patterns are formed by etching the silicon nitride layer (col. 2, ll. 56-58). The surface of the polycrystalline silicon layer is exposed by etching the

interlayer oxide layer using the silicon nitride layer patterns as an etch mask, thereby forming a plurality of interlayer oxide layer patterns (col. 2, ll. 58-62). Thereafter, Ahn forms sidewall spacers on the sidewalls of silicon nitride layer patterns and interlayer oxide layer patterns (col. 2, ll. 62-64). A mask layer is then formed on an exposed region of the polycrystalline silicon layer (col. 2, ll. 64-66). The silicon nitride layer patterns and the sidewall spacers are removed, and the isolation regions are exposed by etching the polycrystalline silicon layer using the interlayer oxide layer pattern and the mask layer as an etch mask (col. 2, l. 66-col. 3, l. 3).

However, Ahn is silent with regard to spacers comprising polymers resulting from the patterning of a sacrificial layer. Instead, Ahn discloses silicon nitride sidewall spacers 660 (FIGS. 4B-4C and col. 5, ll. 30-35) and forming sidewall spacers 780 in the sidewalls of the silicon nitride layer pattern 770 and the upper oxide layer pattern 762 after the upper oxide layer 760 is etched using the silicon nitride layer pattern 770 as an etch mask (FIGS. 5B-5C and col. 6, ll. 37-44). As a result, Ahn cannot disclose or suggest removing an underlying (or lower) insulating layer using an etching mask including spacers comprising polymers resulting from the patterning of a sacrificial layer, as presently claimed.

Keller teaches a method for etching nitride features in [an] integrated circuit construction (Title). The method involves two or three steps (Abstract, ll. 1-2, and col. 3, ll. 63-66), and generally comprises selecting a process chemistry to set a predetermined critical dimension bias; conducting a primary etch of the process chemistry which will have a high etch rate; and conducting a secondary etch of ion bombardment having a lower etch rate and high selectivity to pad oxide (Abstract, ll. 2-7). In selecting the process chemistry, selecting greater amounts of CHF_3 will result in higher polymer concentration on the etched sidewall, and varying the pressure and power can also be used to vary the polymer concentration (Abstract, ll. 7-11). This in turn is used to select the desired critical dimension bias (Abstract, ll. 11-12). The secondary etch uses a mixture of NF_3 and HBr and is performed at a high pressure and a low power to promote high nitride to oxide selectivity (Abstract, ll. 12-14). The secondary etch ***removes the majority of polymer from the nitride sidewalls*** and cleans the polymer from the chamber walls (Abstract, ll. 14-18; emphasis added).

To further emphasize the importance of removing the polymer from the sidewalls of the nitride pattern, Keller explicitly teaches that during the final etch of the second step, some of the polymer will be etched off the sidewalls of the nitride features, as a kind of over etch of the polymer (col. 7, ll. 29-31). The desired result of the over etch of the polymer is shown in FIG. 5, in which the sidewalls of nitride feature 18 are left with a slight coating of polymer 20 and which will maintain the desired critical dimension bias, which will be preferably zero (col. 7, ll. 35-40; see also col. 8, ll. 35-43). This "over etch" of the sidewall polymer is performed before any subsequent processing (although Keller appears to largely silent with regard to appropriate subsequent processing steps; see, e.g., col. 8, ll. 62-67).

As a result, Keller cannot possibly suggest to one of ordinary skill in the art that spacers comprising polymers resulting from the patterning of a sacrificial layer could be useful as part of an etching mask in removing an underlying (or lower) insulating layer, as is presently claimed. Consequently, no combination of Ahn and Keller can teach, disclose or suggest to one of ordinary skill in the art the step of removing an underlying (or lower) insulating layer using an etching mask including spacers comprising polymers resulting from the patterning of a sacrificial layer, as presently claimed.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 3 under 35 U.S.C. § 103

The rejection of Claim 3 under 35 U.S.C. § 103 as being unpatentable over Ahn in view of Keller and Yu et al. is respectfully traversed.

Claim 3 generally recites the same or substantially similar limitations as amended Claim 1 above. Thus, for essentially the same reasons as for amended Claim 1, Claim 3 is patentable over the cited references.

Yu et al. disclose a method for forming insulator filled, shallow trench isolation regions, with rounded corners, using a polymer coated opening in an insulator layer as a mask to define the shallow trench region in silicon (Abstract, ll. 1-5). However, it is quite clear that Yu et al. do

not use spacers comprising polymers as an etching mask in removing an underlying (or lower) insulating layer.

For example, Yu et al. use an anisotropic RIE procedure to transfer opening 5a in photoresist layer 4 to the underlying insulator layers (i.e., silicon nitride layer 3 and pad oxide layer 2; see col. 3, ll. 10-15 and FIG. 1). A thin polymer layer 6a is formed on the top of photoresist shape 4 as well as on the sides of opening 5a (col. 3, ll. 15-16), including on the side of pad oxide layer 2 (FIG. 1). As a result, Yu et al. cannot use spacers comprising polymers as an etching mask ***in removing an insulating layer underlying a sacrificial layer.***

Thus, Yu et al. cannot cure the salient deficiencies of Ahn and Keller with regard to amended Claim 1, which recites the step of removing an underlying (or lower) insulating layer using an etching mask including spacers comprising polymers resulting from the patterning of a sacrificial layer. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

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If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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